REMARKS

Claims 1-11, 13-15, and 29-46 are currently pending in the application. By this amendment, claims 36, 38, and 39 are amended for the Examiner's consideration. The above amendments do not add new matter to the application and are fully supported by the original disclosure. For example, support for the amendments is provided in the claims as originally filed and at Figures 1-5. Reconsideration of the rejected claims in view of the above amendments and the following remarks is respectfully requested.

Allowed Claims

Applicants appreciate the indication that claims 13-15 and 32-34 contain allowable subject matter. However, Applicants submit that all of the claims are in condition for allowance for the following reasons.

35 U.S.C. §102 Rejection

Claims 1-7 were rejected under 35 U.S.C. §102(b) for being anticipated by U. S. Patent No. 6,248,637 issued to Yu ("Yu"). Claims 29-31 were rejected under 35 U.S.C. §102(b) for being anticipated by U. S. Patent No. 5,955,770 issued to Chan et al. ("Chan"). These rejections are respectfully traversed.

To anticipate a claim, each and every element as set forth in the claim must be found, either expressly or inherently described, in a single prior art reference. MPEP §2131. Applicants submit that the references supplied by the Examiner do not show each and every feature of the claimed invention.

Claims 1-7 in view of Yu

The invention generally relates to a semiconductor device and method of manufacture and, more particularly, to a semiconductor device that includes strained silicon/silicon germanium field effect transistors with a protective silicon layer. In non-limiting exemplary embodiments of the invention, a strained silicon layer 155 is provided over a raised source (or drain) 160 (FIG. 4). Moreover, a protective silicon layer 400 is provided over the strained silicon layer 155 and sides of the raised source 160. The protective silicon layer 400 comprises a cap portion 430 and sidewall portions 410, 420 (FIG. 4). In even further embodiments, sacrificial oxide spacers 505, 525 may be used to limit the thickness of the silicon layer sidewalls 510, 520 (FIG. 5). Following the formation of the silicon sidewalls and cap, silicide contacts may be formed on the silicon layer. Independent claim 1 recites, in part:

> forming a first silicon layer over the raised source region and a second silicon layer over the raised drain region,
>
> wherein the first silicon layer formed over the raised source region and the second silicon layer over the raised drain region include cap portions and sidewall portions, the method further comprising a step of forming sacrificial spacers along the silicon sidewall portions.

Yu does not disclose these features. The Examiner asserts that Yu shows forming a first silicon layer 53 over a raised source region 22 and a second silicon layer 53 over a raised drain region 24. The Examiner further asserts that the silicon layer 53 includes cap and sidewall portions. Applicants respectfully disagree and submit that Yu does not contain these features.

Yu shows a process for manufacturing transistors having raised source and drain regions. After formation of the gate structure 18 on the substrate 14, layer 53 is epitaxially grown on the substrate 14 (FIG. 4). Subsequently, layer 53 and the top portion of the substrate are selectively doped to create the source and drain regions 22, 24 (FIG. 5). The source and drain 22, 24 are formed after layer 53. Thus, contrary to the Examiner's assertion, it is impossible for layer 53 to constitute a silicon layer that is formed over the raised source region. Put another way, the order of the steps of Yu's manufacturing process is different from that which is necessarily implied by the language of claim 1. That is, the language of claim 1, by reciting that the first silicon layer is formed over the raised source region, necessarily requires that the raised source and drain be formed before the silicon layer. Yu discloses the opposite: that the source and drain 22, 24 are formed after the silicon layer 53. Therefore, Yu does not disclose forming a first silicon layer over the raised source region and a second silicon layer over the raised drain region, as recited in claim 1.

Furthermore, even assuming *arguendo* that layer 53 constitutes a silicon layer that is formed over a raised source region, which Applicants do not concede, layer 53 does not comprise a cap portion and sidewall portions. Instead, layer 53 merely comprises a block (see, for example, FIGS. 4 and 5). The block structure of layer 53 does not constitute a cap portion and sidewall portions, as recited in claim 1. Therefore, Yu does not contain all of the features of claim 1.

Regarding claims 2-7, Applicants submit that these claims depend from allowable independent claim 1 and are allowable for at least the reasons discussed above.

Moreover, Applicants submit that Yu does not disclose many of the features of the dependent claims.

For example, Yu does not disclose that the substrate includes a SiGe layer atop a buried oxide layer, as recited in claim 2. The Examiner asserts that Yu discloses these features in the paragraph that spans columns 3 and 4. Applicants respectfully disagree. Yu discloses that the substrate may comprise P-type silicon (col. 3, lines 66-67). Yu discloses that the substrate may alternatively be gallium arsenide, or germanium, or semiconductor-on-insulator (SOI). Yu does not explicitly disclose that the substrate comprises a SiGe layer, and none of the four disclosed alternatives necessarily comprises SiGe. Furthermore, Yu does not explicitly disclose that the substrate comprises a buried oxide layer, and none of the four disclosed alternatives necessarily comprises a buried oxide layer. Even further, because Yu does not disclose either SiGe or a buried oxide layer, it is impossible for Yu to disclose a SiGe layer atop a buried oxide layer. Therefore, Yu does not contain all of the features of claim 2.

Accordingly, Applicants respectfully request that the rejection over claims 1-7 be withdrawn.

Claims 29-31 in view of Chan

Independent claim 29 recites, in pertinent part:

> forming a strained silicon layer on the raised source region and the raised drain region; and
> forming a silicon cap on the strained silicon layer.

Chan does not disclose these features. The Examiner asserts that Chan discloses forming a strained silicon layer 80 on a raised source/drain region 77, and forming a silicon cap 82 on the strained silicon layer 80. Applicants respectfully disagree and submit that Chan does not contain these features.

Similar to Yu, Chan discloses epitaxially growing a silicon layer 80 on a substrate 50. After layer 80 is grown, ions are implanted in layer 80 to create the source and drain regions 77. The source and drain 77 are formed after layer 80. Thus, contrary to the Examiner's assertion, layer 80 is not formed on a raised source/drain region because the source and drain do not yet exist when layer 80 is grown. As such, the order of the steps of Chan's manufacturing process is different from that which is necessarily implied by the language of claim 29. That is, the language of claim 29, by reciting that the strained silicon layer is formed on the raised source region, necessarily requires that the raised source and drain be formed before the strained silicon layer. Chan discloses the opposite: that the source and drain 77 are formed after the layer 80. Therefore, Chan does not disclose forming a strained silicon layer on the raised source region and the raised drain region, as recited in claim 29.

Moreover, there is no indication in Chan that layer 80 comprises strained silicon. Therefore, Chan does not disclose forming a strained silicon layer on the raised source region and the raised drain region, as recited in claim 29.

Furthermore, layer 82 is a silicide layer, not a silicon layer as asserted by the Examiner. Applicants submit that silicon and silicide have recognized different meanings to those of skill in the art. For example, Applicants note that, in the instant invention, silicide contacts are formed on the silicon layer following formation of the

silicon layer. Therefore, the skilled artisan recognizes that silicide is not silicon, and that Chan does not disclose forming a silicon cap on the strained silicon layer, as recited in claim 29.

Regarding claims 30 and 31, Applicants submit that these claims depend from allowable independent claim 29 and are allowable for at least the reasons discussed above. Moreover, Applicants submit that Yu does not disclose many of the features of the dependent claims.

Accordingly, Applicants respectfully request that the rejection over claims 29-31 be withdrawn.

35 U.S.C. §103 Rejection

Claims 8-11 were rejected under 35 U.S.C. §103(a) for being unpatentable over Yu in view of U. S. Patent No. 6,939,751 issued to Zhu et al. ("Zhu"). Claims 35-46 were rejected under 35 U.S.C. §103(a) for being unpatentable over Chan in view of Zhu. These rejections are respectfully traversed.

Applicants note that both of the above-noted rejections under 35 U.S.C. §103(a) (i.e., that of claims 8-11 and that of claims 35-46) are based at least in part upon the Zhu reference.

However, Applicants submit that, pursuant to 35 U.S.C. §103(c), Zhu cannot be applied against the pending claims under 35 U.S.C. §103(a). Under 35 U.S.C. §103(c), subject matter developed by another person, which qualifies as prior art only under one of 35 U.S.C. §§102(e), (f), or (g) shall not preclude patentability under 35 U.S.C. §103

where the subject matter and the claimed invention were, at the time the invention was made, commonly owned.

Applicants note that Zhu only qualifies as prior art under 35 U.S.C. §102(e) because Zhu was issued September 6, 2005 (i.e., after the U.S. filing date of the present application) and was filed October 23, 2003 (i.e., before the U.S. filing date of the present application). Therefore, Zhu qualifies as prior art only under 35 U.S.C. §102(e).

Applicants further note that the instant application and Zhu are both assigned to International Business Machines Corporation (IBM). Moreover, Applicants submit that the invention of the instant application and Zhu were commonly owned by IBM or subject to an obligation of assignment to IBM at the time the invention was made, as evidenced by the assignment recorded by the USPTO at Reel 014065 and Frame 0095 on October 22, 2003 for Zhu, and the fact that the invention was subject to an obligation assignment to IBM at the time the invention was made.

Therefore, because Zhu only qualifies as prior art under 35 U.S.C. §102(e) and because Zhu and the instant invention were commonly owned at the time the invention was made, Zhu cannot be used to preclude the patentability of claims 8-11 and 35-46 under 35 U.S.C. §103.

Accordingly, Applicants respectfully request that the rejection over claims 8-11 and 35-46 be withdrawn.

Other Matters

Claims 36, 38, and 39 have been amended to correct typographical errors that have come to Applicants' attention.

CONCLUSION

In view of the foregoing amendments and remarks, Applicants submit that all of the claims are patentably distinct from the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue. The Examiner is invited to contact the undersigned at the telephone number listed below, if needed. Applicants hereby make a written conditional petition for extension of time, if required. Please charge any deficiencies in fees and credit any overpayment of fees to Attorney's Deposit Account No. 09-0458.

Respectfully submitted,
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